FORM-PTO-1390 (Rev. 12-29-99) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 09/857290
032326-144

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5): Unassigned

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR99/02694	4 November 1999	12 December 1998

TITLE OF INVENTION: CHIP CARD LOADABLE WITH COMPRESSED DATA

APPLICANT(S) FOR DO/EO/US: Benoît BRIEUSSEL

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and the PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information:

JC05 Rec'd PCT/PTO 01 JUN 2001

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5(a))	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
Unassigned 09/857290	PCT/FR99/02694	032326-144

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1,000.00 (960)		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $860.00 (970)		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00 (958)		
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) $690.00 (956)		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00 (962)		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of **$130.00 (154)** for furnishing the oath or declaration later than 20 ☐ 30 ☐ months from the earliest claimed priority date (37 CFR 1.492(e)).	$ -0-	

Claims	Number Filed	Number Extra	Rate		
Total Claims	20 -20 =	-0-	X$18.00 (966)	$ -0-	
Independent Claims	3 -3 =	-0-	X$80.00 (964)	$ -0-	
Multiple dependent claim(s) (if applicable)			+$270.00 (968)	$ -0-	
TOTAL OF ABOVE CALCULATIONS =				$ 860.00	
Reduction for 1/2 for filing by small entity, if applicable (see below).				$ -0-	-
SUBTOTAL =				$ 860.00	
Processing fee of **$130.00 (156)** for furnishing the English translation later than 20 ☐ 30 ☐ months from the earliest claimed priority date (37 CFR 1.492(f)). +				$ -0-	
TOTAL NATIONAL FEE =				$ -0-	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00 (581)** per property +				$ -0-	
TOTAL FEES ENCLOSED =				$ 860.00	
				Amount to be: refunded	$
				charged	$

a. ☐ Small entity status is hereby claimed.

b. ☒ A check in the amount of $ 860.00 to cover the above fees is enclosed.

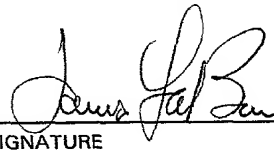
c. ☐ Please charge my Deposit Account No. 02-4800 in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

d. ☐ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-4800. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

James A. LaBarre
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620



SIGNATURE

James A. LaBarre
NAME

28,632
REGISTRATION NUMBER

Patent
Attorney's Docket No. 032326-144

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Benoît BRIEUSSEL	)	Group Art Unit: Unassigned
	)	
Application No.: Unassigned	)	Examiner: Unassigned
	)	
Filed: June 1, 2001	)	
	)	
For: CHIP CARD LOADABLE WITH COMPRESSED DATA	)	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination and the calculation of filing fees, kindly amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 1, immediately following the title appearing on line 1, insert the following:

--This disclosure is based upon, and claims priority from French Application No. 98/15257, filed on December 1, 1998 and International Application No. PCT/FR99/02694, filed November 4, 1999, which was published on June 8, 2000 in a language other than English, the contents of which are incorporated herein by reference.

Background of the Invention--

Page 3, between lines 4 and 5, insert the following heading:

--**Summary of the Invention** --.

Page 8, between lines 26 and 27, insert the following heading:

--**Brief Description of the Drawings**--.

Page 9, between lines 18 and 19, insert the following heading:

--**Detailed Description**--.

Add the following Abstract:

--The invention concerns a chip card receiving fields of compressed data encapsulated in frames including an indication of the expected length of decompressed data and a length of compressed data. The frames are received in a storage unit and the processor of the card decompresses each data field according to a decompression algorithm over a length based on the indication of the expected length and writes the decompressed data in another buffer storage unit. Several algorithms and optionally several decompression models are installed in the card storage unit, and a couple thereof is selected by the number read in the heading of each frame received.--

IN THE CLAIMS:

Kindly replace claims 1-20, as follows.

1. A chip card that receives compressed data fields each preceded by an indication of the expected length of decompressed data and a length of compressed data, comprising a first memory for storing the received fields of compressed data according to the lengths of the respective compressed data, a second memory for storing a decompression algorithm, a processor for decompressing, according to said decompression algorithm, the compressed data in each field into decompressed data over a length depending on the indication of length of decompressed data, and a third memory for storing the decompressed data.

2. A chip card according to Claim 1, in which the second memory contains several decompression algorithms, and the processor detects a decompression algorithm number preceding each received field of compressed data so that the compressed data is decompressed in accordance with the decompression algorithm whose number has been detected.

3. A chip card according to Claim 2, in which the second memory comprises several decompression models respectively associated with the decompression algorithms, and the processor detects a decompression model number preceding each received field of compressed data so that the compressed data is decompressed in accordance with the

corresponding decompression algorithm and decompression model whose numbers have been detected.

4. A chip card according to Claim 2, comprising a fourth memory for storing a decompression model received previously to a received compressed data field, and wherein said processor detects the number of a decompression algorithm preceding said received field of compressed data so that the compressed data is decompressed according to the decompression algorithm whose number has been detected and the decompression model stored in the fourth memory.

5. A chip card according to Claim 2, comprising a fourth memory for storing a decompression model implicitly deduced from a compressed data field during writing in the first memory, and the processor detects the number of a decompression algorithm preceding said stored field of compressed data so that the compressed data is decompressed according to the decompression algorithm whose number was detected and the derived decompression model stored in the fourth memory.

6. A chip card according to claim 1, wherein said processor detects an indication of the compressed or non-compressed state of each received data field so that the processor decompresses the data only in the data fields preceded by an indication of a compressed state.

7. A protocol data unit for a chip card that receives compressed data fields, comprising a header and a data field, the header including the length of the data field and an indication of the expected decompressed data length after decompression of the data field.

8. A protocol data unit according to Claim 7, in which the indication of the expected decompressed data length is an n-bit word equal to the expected length of the decompressed data modulo 2^n, the expected length being expressed in decompressed m-bit data words, with n being an integer equal to at least 0 and m being an integer equal to at least 1.

9. A protocol data unit according to Claim 7, in which the header further includes the number of a decompression algorithm by means of which the data compressed in the data field is to be decompressed.

10. A protocol data unit according to Claim 9, in which the header further includes the number of a decompression model which corresponds to the decompression algorithm whose number is included in the header and by means of which the compressed data in the data field is to be decompressed.

11. A protocol data unit according to Claim 7, in which the header includes a data state indication having a first state when the data in the data field are not compressed, and having a second state when the data in the data field are compressed.

12. A protocol data unit according to Claim 11, in which the data state indication has a third state when the data in the data field are to be decompressed in accordance with a predetermined decompression algorithm and a predetermined decompression model.

13. A protocol data unit according to Claim 11, in which the header comprises the number of a decompression algorithm, the number of a decompression model and the indication of the expected decompressed data length when the data state indication is at the second state.

14. A method for decompressing compressed data fields in a chip card, each compressed data field being preceded by an indication of the expected decompressed data length corresponding to compressed data contained in the field and by a length of the compressed data contained in the field, comprising the following steps:

- detecting the length of the compressed data and storing the compressed data field over the detected length, and

- detecting the indication of the expected decompressed data length and decompressing the data so as to stop the decompression according to the detected indication.

15. A method according to Claim 14, further including the steps of selecting a decompression algorithm amongst several decompression algorithms according to the

number of an algorithm preceding the compressed data field, and decompressing the data in the field in accordance with the selected decompression algorithm.

16. A method according to Claim 15, further including the steps of selecting a decompression model amongst several decompression models associated with the selected decompression algorithm according to the number of a model preceding the compressed data field, and compressing the data in the field in accordance with the decompression algorithm selected and the decompression model selected.

17. A method according to Claim 15, further including the steps of storing a decompression model received previously in the compressed data field, and decompressing the data in the field in accordance with the selected decompression algorithm and the stored decompression model.

18. A method according to Claim 15, further including the steps of storing a decompression model deduced implicitly from the received compressed data field, and decompressing the data in the field in accordance with the selected decompression algorithm and the deduced and stored decompression model.

19. A method according to Claim 14, further including the step of detecting a data state indication preceding each received data field in order to decompress the data in the field only when the data state indication is not at a first predetermined state.

20. A method according to Claim 19, wherein the step of detecting an indication of the expected decompressed data length is not performed when the data state indication is at a predetermined state indicating that the compressed data are to be decompressed according to a predetermined algorithm and model.

REMARKS

Entry of the foregoing amendment is respectfully requested. This amendment is intended to place the claims in a more conventional format and eliminate the multiple dependency of the claims.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: 

James A. LaBarre
Registration No. 28,632

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

Date: June 1, 2001

Attachment to Preliminary Amendment dated June 1, 2001

Marked-up Claims 1-20

1. (Amended) A chip card [(CA, SIM) able to receive] that receives compressed data fields [(DATA)] each preceded by an indication of the expected length of decompressed data [(LDD)] and a length of compressed data [(LC), is characterised in that it comprises a first means (MC)], comprising a first memory for storing the received fields of compressed data [(DATA, TR)] according to the lengths of the respective compressed data [(LC), a second means (MS)], a second memory for storing a decompression algorithm, a [means (PR)] processor for decompressing, according to [the] said decompression algorithm, the compressed data in each field [and] into decompressed data over a length depending on the indication of length of decompressed data [(LDD)], and a third [means (MD)] memory for storing the decompressed data.

2. (Amended) A chip card according to Claim 1, in which the second [storage means (MS)] memory contains several decompression algorithms [(AL0 to ALi)], and the [decompression means (PR)] processor detects a decompression algorithm number [(ALi)] preceding each received field of compressed data so that [these are] the compressed data is decompressed in accordance with the decompression algorithm whose number has been detected.

3. (Amended) A chip card according to Claim 2, in which the second [storage means (MS)] memory comprises several decompression models [(Mi0) to MiJ)] respectively

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Marked-up Claims 1-20

associated with the decompression algorithms [(AL0 to ALI)], and the [decompression means (PR)] processor detects a decompression model number [(Mij)] preceding each received field of compressed data so that [these are] the compressed data is decompressed in accordance with the corresponding decompression algorithm and decompression model whose numbers have been detected.

4. (Amended) A chip card according to Claim 2, comprising a fourth [means (MM)] memory for storing a decompression model received previously to a received compressed data field, and [the decompression means (PR)] wherein said processor detects the number of a decompression algorithm [(ALi)] preceding [the] said received field of compressed data so that [these are] the compressed data is decompressed according to the decompression algorithm whose number has been detected and the decompression model [read] stored in the fourth storage means (MM)] memory.

5. (Amended) A chip card according to Claim 2, comprising a fourth [means (MM)] memory for storing a decompression model implicitly deduced from a compressed data field during writing in the first [storage means (MC)] memory, and the [decompression means (PR)] processor detects the number of a decompression algorithm [(ALi)] preceding [the] said stored field of compressed data so that [these are] the compressed data is decompressed according to the decompression algorithm whose number was detected and

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Marked-up Claims 1-20

the derived decompression model [read] stored in the fourth [storage means (MM)] memory.

6. (Amended) A chip card according to [any one of Claims 1 to 5, in which the decompression means (PR)] claim 1, wherein said processor detects an indication [(CLA: B2, B3) on] of the compressed or non-compressed state of each received [compressed] data field so that the [decompression means (PR)] processor decompresses the data only in the data fields preceded by an indication of a compressed state.

7. (Amended) A protocol data unit for [being received notably by the chip card according to any one of Claims 1 to 6] a chip card that receives compressed data fields, comprising a header [(ET)] and a data field [(DATA)], the header including the length [(LC)] of the data field[, characterised in that the header (ET) comprises] and an indication [(LDD) on] of the expected decompressed data length after decompression of the data field [(DATA)].

8. (Amended) A protocol data unit according to Claim 7, in which the indication [on] of the expected decompressed data length [(LDD)] is an n-bit word equal to the expected length of the decompressed data modulo 2^n, the expected length being

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Marked-up Claims 1-20

expressed in decompressed m-bit data words, with n being an integer equal to at least 0 and m being an integer equal to at least 1.

9. (Amended) A protocol data unit according to Claim 7 [or 8], in which the header [(ET) comprises] further includes the number [(ALi)] of a decompression algorithm by means of which the data compressed in the data field [(DATA) are] is to be decompressed.

10. (Amended) A protocol data unit according to Claim 9, in which the header [(ET) comprises] further includes the number [(Mij)] of a decompression model which corresponds to the decompression algorithm whose number [(ALi)] is included in the header and by means of which the compressed data in the data field [(DATA) are] is to be decompressed.

11. (Amended) A protocol data unit according to [any one of Claims 7 to 10] Claim 7, in which the header [(ET)] includes a data state indication [(B1, B2)] having a first state [(DATA)] when the data in the data field are not compressed, and having a second state when the data in the data field [(DATA)] are compressed.

12. (Amended) A protocol data unit according to Claim 11, in which the data state indication [(B1, B2)] has a third state when the data in the data field [(DATA)] are to

Attachment to Preliminary Amendment dated June 1, 2001

Marked-up Claims 1-20

be decompressed in accordance with a predetermined decompression algorithm [(AL0)] and a predetermined decompression model [(M00)].

13. (Amended) A protocol data unit according to Claim 11 [or 12], in which the header [(ET)] comprises the number of a decompression algorithm [(ALi)], the number of a decompression model [(Mij)] and the indication [on] <u>of</u> the expected decompressed data length [(LDD)] when the data state indication [(B1, B2)] is at the second state.

14. (Amended) A method for decompressing compressed data fields [(DATA) to be implemented notably in the chip card according to any one of Claims 1 to 6] <u>in a chip card</u>, each compressed data field being preceded by an indication [on] <u>of</u> the expected decompressed data length [(LDD)] corresponding to compressed data contained in the field and by a length [(LC)] of the compressed data contained in the field, [characterised by] <u>comprising</u> the following steps:

- detecting [(D3)] the length [(LC)] of the compressed data and storing [(D0)] the compressed data field [(DATA)] over the detected length, and

- detecting [(D8)] the indication [on] <u>of</u> the expected decompressed data length [(LDD)] and decompressing [(D9)] the data so as to stop the decompression according to the detected indication [(LDD)].

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Marked-up Claims 1-20

15. (Amended) A method according to Claim 14, [comprising a step (D6)] further including the steps of selecting a decompression algorithm [(ALi)] amongst several decompression algorithms [(AL0 to ALI)] according to the number of an algorithm preceding the compressed data field [in order to decompress], and decompressing the data in the field in accordance with the selected decompression algorithm.

16. (Amended) A method according to Claim 15, [comprising a step (D7, D72)] further including the steps of selecting a decompression model [(Mij)] amongst several decompression models [(Mi0 to MiJ)] associated with the selected decompression algorithm [selected] according to the number of a model preceding the compressed data field [in order to decompress], and compressing the data in the field in accordance with the decompression algorithm selected and the decompression model selected.

17. (Amended) A method according to Claim 15, [comprising a step (D71)] further including the steps of storing a decompression model [(Mij)] received previously in the compressed data field [(DATA) in order to decompress], and decompressing the data in the field in accordance with the selected decompression algorithm and the stored decompression model.

Attachment to Preliminary Amendment dated June 1, 2001

Marked-up Claims 1-20

18. (Amended) A method according to Claim 15, [comprising a step (D71)] further including the steps of storing a decompression model [(Mij)] deduced implicitly from the received compressed data field [(DATA) in order to decompress], and decompressing the data in the field in accordance with the selected decompression algorithm and the deduced and stored decompression model.

19. (Amended) A method according to [any one of Claims 14 to 18, comprising a step (D4, D50, D51, D52)] Claim 14, further including the step of detecting a data state indication [(B2, B3)] preceding each [decompressed] received data field in order to decompress the data in the field only when the data state indication is not at a first predetermined state.

20. (Amended) A method according to Claim 19, [according to which] wherein the step [(D8)] of detecting an indication [on] of the expected decompressed data length [(LDD)] is not performed when the data state indication [(B2, B3)] is at a predetermined state indicating that the compressed data are to be decompressed according to a predetermined algorithm and model [(AL0, M00)].

Chip card loadable with compressed data

The invention relates in general terms to the processing of data received in a chip card, also referred to as a microcomputer or microprocessor card (smart card).

The service providers managing chip cards have a greater and greater requirement to store a large number of data in the non-volatile memory of the EEPROM or Flash EEPROM type contained in the chip card. The memory capacity requirements of chip cards also have a tendency to increase because of the use of certain software packages written in programming languages, such as Java, for which parts of programs, such as applets, are to be downloaded into the cards.

In order to give an idea, if 5 kilobytes are transmitted in each of 1 million cards with a single terminal operating 24 hours a day and 7 days a week and whose output is 9600 bits/second, more than 2 months are needed to load these data into the cards.

In radiotelephony, the chip card is integrated as an SIM (Subscriber Identity Module) in the portable radiotelephone terminals. The active state of the radiotelephone terminal and therefore its current consumption and its battery life depend notably on the time taken to transmit the data to be processed by the SIM card.

In more general terms, the reduction in the time taken for transmission of the data to be downloaded into the chip cards is an indisputable gain vis-à-vis both the terminal loading the data into the chip card and vis-à-vis the card itself and the transmission support(s) or channel(s) conveying the data to be downloaded.

In addition the Japanese patent application 08235329 filed on 24 February 1995 proposes downloading compressed data into a memory card, that is to say a "static" card which does not process the data which it receives and serves as a remote memory with respect to an image processing unit which produced the compressed data. The image processing unit writes to two first predetermined addresses in the memory card respectively the length of the data before compression and the length of the data after compression, and then writes the compressed data in the memory card. Conversely, when the compressed data are loaded from the memory card into the image processing unit, the image processing unit reads the length of the data before compression and the length of the data after compression at the respective two aforementioned

addresses, and then reads the compressed data so as to decompress them in accordance with a predetermined decompression algorithm installed in the image processing unit.

The objective of the invention is to reduce the time taken for downloading the data into the chip cards, that is to say the microcomputer or microprocessor cards, by loading compressed data therein, whilst preserving the functionalities of the chip cards with regard to the processing of non-compressed data.

To this end, a chip card able to receive compressed data fields each preceded by an indication of the expected length of decompressed data and a length of compressed data, is characterised in that it comprises a first means for storing the received fields of compressed data according to the lengths of the respective compressed data, a second means for storing a decompression algorithm, a means for decompressing, according to the said decompression algorithm, the compressed data in each field and decompressed data over a length depending on the indication of length of decompressed data, and a third means for storing the decompressed data.

By virtue of the reception of data in the compressed state in the chip cards according to the invention, the time taken for loading 5 kilobytes into a million of these cards according to the aforementioned example is reduced by 10% to 40%,

typically by 20%, giving a saving of approximately two weeks.

Preferably, the second storage means contains several decompression algorithms and the decompression means detects the number of a decompression algorithm preceding each received field of compressed data so that these are decompressed according to the decompression algorithm whose number has been detected. In a variant, the second storage means can comprise several decompression models respectively associated with the decompression algorithm, and the decompression means detects the number of a decompression model preceding each received field of compressed data so that these are decompressed according to the decompression algorithm and the corresponding decompression model whose numbers have been detected. The various decompression algorithms and decompression models installed in memory in the card enable the card to be used by any service provider managing the terminals or servers compressing data according to one of the algorithms and one of the models.

According to another characteristic of the invention, the chip card comprises a fourth means for storing a decompression model received previously to a received compressed data field, and the decompression means detects a number of a decompression algorithm preceding the said received field of compressed data so that these are decompressed according to the decompression algorithm whose number has been detected

and the decompression model read in the fourth storage means.

According to another possibility, the decompression model is reconstructed in the RAM memory of the card; in this case, the fourth storage means stores a decompression model derived implicitly from a compressed data field during writing in the first storage means, and the decompression means detects the number of a decompression algorithm preceding the said stored field of compressed data so that these are decompressed according to the decompression algorithm whose number was detected and the derived decompression model read in the fourth storage means.

The decompression means can detect an indication on the compressed or non-compressed state of each received field of compressed data so that the decompression means decompresses the data only in the data fields preceded by an indication of compressed state.

The invention also relates to a protocol data unit for being received notably by the chip card according to the invention. The unit comprises a header and a data field, the header including the length of the data field, and is characterised in that the header comprises an indication on the expected length of decompressed data after decompression of the data field. This characteristic helps to decompress precisely, whatever the decompression algorithm selected.

The indication on the expected length of decompressed data is an n-bit word equal to the expected length of the decompressed data modulo 2^n, the expected length being expressed in m-bit words of decompressed data. The integer n is equal to at least 0, for example equal to 2, 3 or 4 bits according to the distribution of decompression parameters in a field of the protocol unit. The integer m is equal to at least 1, for example equal to 8 for words such as bytes.

When the card is of the multi service provider type, the header includes the number of a decompression algorithm by means of which the compressed data in the data field are to be decompressed, and may include the number of a decompression model which corresponds to the decompression algorithm whose number is included in the header and by means of which the compressed data in the data field are to be decompressed.

The card can receive compressed data and non-compressed data.

To this end, the header comprises a data state indication having a first state when the data in the data field are not compressed, and having a second state when the data in the data field are compressed. The data state indication can have a third state when the data in the data field are to be decompressed according to a predetermined decompression algorithm and a predetermined decompression model which can be chosen by default in the card; the indication on the expected length of decompressed data is then not always necessary for decompression and may not be in the

protocol data unit. In the contrary case, the header comprises the number of a decompression algorithm, the number of a decompression model and an indication on the expected length of decompressed data when the data state indication is at the second state.

Finally, the invention also relates to a method for decompressing compressed data fields to be implemented notably in the chip card according to the invention. Each compressed data field is preceded by an indication on the length of non-compressed data corresponding to compressed data contained in the field and a length of compressed data contained in the field. The method is characterised by the following steps:

- detecting the length of compressed data and storing the compressed data field over the detected length, and

- detecting the indication of the expected length of decompressed data and decompressing the data so as to stop the decompression according to the detected indication.

The method can comprise, for a multi service provider application, a step of selecting a decompression algorithm amongst several decompression algorithms according to the number of an algorithm preceding the compressed data field in order to decompress the data in the field following the selected decompression algorithm, and where applicable a step of selecting a decompression model amongst several decompression models associated with the decompression algorithm selected according to the number of a model

preceding the compressed data field in order to decompress the data in the field according to the selected decompression algorithm and the selected decompression model.

In place of the step of selecting a decompression model, the method can comprise a step of storing a decompression model received previously to the compressed data field in order to decompress the data in the field according to the selected decompression algorithm and the stored decompression model, or a step of storing a decompression model derived implicitly from the received compressed data field in order to decompress the data in the field according to the decompression algorithm selected and the decompression model derived and stored.

The method can also comprise a step of detecting a state indication for data preceding each decompressed data field in order to decompress the data in the field only when the data state indication is not at a first predetermined state.

Preferably, the step of detecting an indication on the expected length of decompressed data is to be performed only when the data state indication is at a predetermined state indicating that the compressed data are to be decompressed according to a predetermined algorithm and model, selected by default in the card.

Other characteristics and advantages of the present invention will emerge more clearly from a reading of the following description of several

preferred embodiments of the invention with reference to the corresponding accompanying drawings, in which:

- Figure 1 is a block diagram of a system for transmission between a chip card according to the invention and a terminal with a data compressor according to a first embodiment;

- Figure 2 is a block diagram of a radiotelephony system between a chip card according to the invention and a server with a data compressor according to a second embodiment;

- Figure 3 is a diagram showing a compressed data frame according to the invention;

- Figure 4 is a diagram of a decompression parameter field included in the frame of Figure 3;

- Figure 5 is an algorithm of a data compression method according to the invention; and

- Figure 6 is an algorithm of a data compression method according to the invention.

According to a first embodiment shown in Figure 1, a card reader terminal TE comprises a data compressor COM for compressing data which it has processed internally, whether or not the terminal is self-contained, or which it has received from a transmission line, for example a subscriber telephone line LT served by a unit automatic exchange CO in the switched telephone network STN or an integrated service digital network ISDN. The compressed data are transmitted in frames TR according to the invention by the terminal to a chip card CA through a transmission medium ST of the cable transmission line or radio type or of the

electrical, magnetic or inductive contact type for example. The chip card decompresses according to the invention the compressed data included in the received frames TR.

Schematically the chip in the card comprises a RAM memory MC for storing the received frames with compressed or non-compressed data, a RAM memory MD for storing the decompressed data, a ROM memory MS including the operating system OS (operating system) of the card and specific applications notably according to the invention a EEPROM memory ME for storing notably data transmission/reception protocols, confidential information and decompressed and non-decompressed data, and a microprocessor PR connected to the memories by a bus B.

According to a second embodiment shown in Figure 2, the card terminal is a mobile radiotelephone terminal TM in a cellular radiotelephony network RT, for example of the GSM 900 or DCS 1800 type. The memory card is a SIM card, that is to say a subscriber identity module with an architecture similar to the card CA shown in Figure 2 and substantially modified and supplemented according to the invention. In order not to overload the mobile terminal TM with software, the latter does not compress the data which it receives in order to transmit them to the SIM card but receives these data already compressed through the traffic channel allocated from the corresponding base station.

In the network RT shown in Figure 2, only the main entities through which the data intended for the SIM

card pass are shown. These entities are a mobile service centre MSC connected to at least one group switching centre CO in the switched telephone network STN and managing communications for visiting mobile terminals, including the terminal TM, which are at a given moment situated in a respective location area; a visitor location register VLR connected to the centre MSC and containing characteristics of the mobile terminals, in fact of the SIM cards, in this location area; a base station controller BSC managing notably the allocation of channels to mobile terminals, the power of base station(s) and intercell transfers for mobile stations; and the base station BTS covering the radio cell in which the terminal TM is situated at the given time.

In this second embodiment, the data compressor COM is included in a compression server SC which is connected to the mobile service centre MSC through a conventional ISDN interface, for example of the T2 2048 kilobits/second type with 30 B information channels and one 64 kilobit/second D channel. All the incoming data to be compressed intended for the mobile terminals situated in the said location area for any communications with fixed terminals in the network STN or the mobile terminals in the radiotelephone network RT are compressed in the server SC before passing through the corresponding controller BSC, base station BTS and mobile terminal TM.

In a variant, the server SC is not connected to the mobile service centre MSC, but is replaced by

compressor servers connected respectively to the base station controllers BSC served by the centre MSC.

Referring now to Figures 3 and 4, a protocol data unit in the form of a frame of compressed data TR to be transmitted from the terminal TE, TM to the card CA, SIM through the transmission medium ST, or from the compression server SC through notably the terminal TM according to Figure 2, has a structure with a header ET and a data field DATA. The frame TR is substantially modified compared with a standard frame of incoming data according to the character by character asynchronous transmission protocol "T = 0". Instead of five bytes, the header ET of the frame TR comprises five bytes CLA, INS, P1, P2 and LC as in a "T = 0" frame and a sixth byte PD containing decompression parameters according to the invention, "taken" from the data field. These six bytes are in hexadecimal code.

As in the "T = 0" frame, the byte CLA designates a class of the instruction contained in the following byte, the byte INS an instruction related to a command of the operating system OS (operating system) of the chip card CA, SIM or related to the security of data for example, the bytes P1 and P2 parameters of the instruction, and the byte LC the length of the data field in the "T = 0" frame expressed in bytes and equal, for the majority of compressed data frames according to the invention, to the length of the field DATA of the frame TR increased by 1 due to the byte PD.

According to the invention, the frame TR contains two data state indication bits B2 and B3, the second

and the third in the byte CLA, which are produced in the compressor COM of the terminal TE or of the server SC in order to indicate principally the compressed or non-compressed state of the data in the field DATA. The data state indication bits B2 and B3 have the following respective binary states:

- "00" when the data are received non-compressed, the frame TR then being a "T = 0" frame with the byte PD as a data byte;

- "10" when the data are received compressed and are to be decompressed in the card according to predetermined compression algorithm AL0 and model M00, the most commonly used, selected by default in the chip card CA, SIM, the frame TR then being a "T = 0" frame when the length of the decompressed data is not necessary for decompression; and

- "11" when the data are received compressed and are to be decompressed in the card according to a selected one ALi amongst several decompression algorithms and a selected one Mij amongst several decompression models adapted to the selected algorithm ALi, the decompression algorithm and model ALi and Mij corresponding to the compression algorithm and model "ALi" and "Mij" used in the terminal TE or the server SC for initially compressing in the data.

Thus, according to the invention, the ROM memory MS of the chip card, which contains mainly the operating system OS of the card, also contains several applications relating to decompression algorithms AL0 to ALi with the index i between 0 and an integer I

typically equal to no more than 3, each algorithm ALi being associated with several respective compression models Mi0 to Mij with the index j between 0 and an integer J typically equal to no more than 7. A decompression model provides a match between the compressed symbols and the non-compressed symbols by means of the decompression algorithm which implements it; for example, a model is based on a tree, a probabilistic table, a dictionary or a list. The identification of the algorithm ALi and the identification of the model Mij serving to decompress the data DATA are indicated to the card CA, SIM respectively by a 2-bit word and a 3-bit word at the start of the decompression parameter byte PD, as shown in Figure 4, when the bits B2 and B3 in the class field CLA are "11". The card CA, SIM of the invention is thus adapted to various decompression algorithms which are respectively chosen by various service providers responsible for the management of sets of terminals TE, or sets of terminals TM with servers SC.

As a variant, the chip card CA (Figure 1), SIM also comprises a RAM memory MM connected to the bus B. Characteristics of a decompression model which are included in incoming command frames (non-compressed) preceding the frames TR with compressed data according to this model, are transmitted by the terminal TE or the server SC through the medium ST and are written in the memory MM by the processor PR. The algorithm implementing this model entered in memory MM will then

be sought in the memory MS by the processor in order to decompress the data.

According to another variant, amongst the algorithms AL0 to ALi, some of them are associated with decompression models whose characteristics are not stored in advance in the ROM memory MS of the card CA, SIM. Such a decompression model is reconstructed by means of the corresponding decompression algorithm in the processor PR along with the writing of the compressed data frame in the memory MC, and is written in the RAM memory MM in order to read it during the decompression of the compressed data. The decompression model is, according to this variant, contained implicitly in the compressed data frame.

The decompression parameter field PD in a compressed data frame contains a last n-bit word LDD which indicates to the card CA, SIM the extracted length of the decompressed data modulo 2^n, where n is an integer greater than or equal to 2. The data which are initially non-compressed in the terminal TE or the server SC to which the decompressed data in the card CA, SIM correspond are processed as m-bit data words, m being an integer greater than or equal to 1. The expected length of the data is expressed as m-bit data words, and the word LDD indicates the number of data words in the last field with no more than 2^n data words in the frame which have been compressed. According to the embodiment illustrated in Figure 4, the integer n is equal to 3, in general greater than or equal to 0, the m-bit words are bytes of decompressed data with m =

8, and the word of expected length of the decompressed data LDD contains 3 bits and is equal to the remainder of the division of the expected length of decompressed data by $2^n = 8$.

By means of the decompressed data length parameter LDD, the processor PR in the chip card CA, SIM stops the decompression of the data just at the end of the received data to be decompressed. For example, according to certain decompression algorithms, such as an algorithm of the Huffman type, several symbols can be coded in an m-bit word, in this case one byte for m = 8. The decompression of the symbols must stop at the end of the decompressed frame, which can occur at the first symbol at the start of the last byte; the following bits at the end of this byte are not data but stuffing bits which are introduced into the card after having precisely counted the number of bits of the decompressed data in accordance with the precision indicated by the parameter LDD in parallel with the compressed data length LC.

According to another variant, the precision of the decompressed data length may attain one bit, when m = 1; for example, for n = 8, the parameter LDD indicates the number of data bits expected in the last byte included in the frame.

The parameter LDD is also useful when several "T = 0" frames, or standard frames of incoming data in accordance with the "T = 1" block by block asynchronous transmission protocol, known as application protocol data units APDU, must be concatenated in order to

constitute a file. The start of a frame must follow on precisely from the end of the previous frame, that is to say the last byte of decompressed data. This file segmentation at the last byte of the previous frame is indicated precisely by the parameter LDD.

Instead of the expected length being expressed by the remainder of the division by 2^n it could be introduced completely into the header of the frame TR according to the invention. However, this introduction would add an additional word in the header ET of the frame TR, the expected length then being able to be greater than $2^8 = 256$ bytes. In addition a third bit would be necessary in the class field CLA in order to give all cases.

A compression method in accordance with the invention is shown in Figure 5. It comprises mainly five steps C0 to C4 performed in the terminal TE or the server SC.

When, in accordance with protocol instructions at step C0, the data incoming into the terminal T or the server SC are not compressed, the bits B2 and B3 are set to the state "00" at a step C30 following on from an initial step C0.

If the incoming data are to be compressed at step C0, the terminal TE or the server SC compresses the incoming data at the following step C1 in accordance with a compression algorithm "ALi" and a corresponding compression model "Mij" preinstalled in the terminal TE or the server SC. If the algorithm "ALi" and the module "Mij" are the predetermined compression

algorithm "AL0" and the predetermined compression model "M00" and if the decompression does not make it necessary at step C21 to know the indication on the decompressed data length LDD in so far as the compression has stopped on an integer number of n-bit data words, the bits B2 and B3 are set respectively to the state "10" at step C31. In the contrary cases, at steps C2 and C21, the parameter LDD is necessary, and the bits B2 and B3 are set to the state "11" at step C32. The decompression parameter field PD is formed with the number ALi and Mij of the algorithm and model which serve for compression of the data and with the expected length of the data before compression, modulo 2^n.

Then, at the following step C4, whether the data are compressed or not compressed, the frame TR to be transmitted is finally formed. Optionally, the whole of the frame, or only the data field DATA, is encoded at a step C5.

As shown in Figure 6, the data decompression in the card PC, SIM comprises nine steps D0 to D10. At the initial step D0, the frame TR received according to an asynchronous transmission is written in the RAM buffer memory MC in the card. Optionally, if the frames TR or the data DATA included in this frame have been encoded in the terminal TE or the server SC, the card processor PR executes a deciphering of each frame received and written in the RAM buffer memory at step D1. The processor PR next validates, at step D2, the received frame TR as a standard frame when the most

significant bit B1 in the field of class CLA is at the "1" state; otherwise, when the frame is received with B1 = "0", the method passes from step D2 to step D10. The length of the data field DATA read in the field LC at step D3 fixes the stoppage of the writing of the data in the memory MC.

At the following step D4, the second and third bits B2 and B3 in the field CLA of the received frame TR are read. If these two bits are equal to "00", as indicated at step D50, no data decompression is executed and the method passes directly to the last step D10. In the contrary case, the data DATA must be decompressed and the method passes to step D51 in order to distinguish the frames without and with a decompression parameter field PD.

If at step D51 the bits B2 and B3 are not respectively equal to "11", they are equal to "10" at step D52. The operating system OS automatically selects the predetermined decompression algorithm and model AL0 and M00 in the memory MS at step D60, and then executes the decompression of the data DATA and writes the decompressed data in the memory MD at step D9. The end of the decompression is estimated according to the length LC of the fields DATA.

When the bits B2 and B3 are respectively "11" at step D51, the operating system OS will select the decompression algorithm and model. The decompression algorithm ALi indicated by the first two bits of the decompression parameter field PD included in the received frame TR is selected in the ROM memory MS of

the card at step D6. The corresponding decompression model Mij is read in the RAM memory MM at steps D7 and D71, if the characteristics of the model Mij were previously received on reception of the frame TR or implicitly deduced at the start of the reception of the frame TR. In the contrary case, the three model bits in the field PD of the received frame are read in order to select the model Mij in the ROM memory MS at steps D7 and D72. Then, after step D71 or D72, the n-bit word LDD at the end of the decompression parameter field PD is read at step D8 by the operating system OS so that, at step D9, the processor PR executes the decompression of the data contained in the field DATA of the received frame TR and stops this decompression according notably to the word LDD read previously. The decompressed data are written as and when in the RAM memory MD.

According to the instruction contained in the field INS and the parameters P1, P2 specifying this instruction in the received frame TR, the operating system OS at step D10 executes a given command, such as for example the copying of the decompressed data contained in the memory MD into the EEPROM memory of the card, at a given file address. At this stage, the operating system in the card is exactly in the situation which it would encounter in a standard card, if the received data had not been compressed according to the invention.

By way of example, the header ET contained in a compressed data frame TR is as follows:

CLA = "E8"; INS = "D0"; P1 = "03"; P2 = "20"; LC = "23" and PD = "B6",

all these bytes being in hexadecimal code.

In this example, the first half of the field CLA is equal to "1110", that is to say B2 = "1" and B3 = "1", which means that the data DATA have been compressed with an algorithm and a model other than the algorithm "AL0" and the model "M00". According to the field LC, the data DATA after compression extend over (16x2+3) = 35 bytes. The decompression is effected according to the algorithm AL2 and the corresponding model M26, whose numbers are read in the first five bits "10110" of the decompression parameter field PD. The expected length of the decompressed data LDD contains an integer number of groups of 8 bytes + 3 bytes according to the last three bits LDD = "011" of the field PD of the frame TR.

In the other transmission direction, from the card CA, SIM to the terminal TE, TM, the data are not initially compressed and are encapsulated by the card in standard frames "T = 0", or possibly "T = 1".

CLAIMS

1. A chip card (CA, SIM) able to receive compressed data fields (DATA) each preceded by an indication of the expected length of decompressed data (LDD) and a length of compressed data (LC), is characterised in that it comprises a first means (MC) for storing the received fields of compressed data (DATA, TR) according to the lengths of the respective compressed data (LC), a second means (MS) for storing a decompression algorithm, a means (PR) for decompressing, according to the said decompression algorithm, the compressed data in each field and decompressed data over a length depending on the indication of length of decompressed data (LDD), and a third means (MD) for storing the decompressed data.

2. A chip card according to Claim 1, in which the second storage means (MS) contains several decompression algorithms (AL0 to ALi), and the decompression means (PR) detects a decompression algorithm number (ALi) preceding each received field of compressed data so that these are decompressed in accordance with the decompression algorithm whose number has been detected.

3. A chip card according to Claim 2, in which the second storage means (MS) comprises several decompression models (Mi0) to MiJ) respectively associated with the decompression algorithms (AL0 to ALI), and the decompression means (PR) detects a decompression model number (Mij) preceding each

received field of compressed data so that these are decompressed in accordance with the corresponding decompression algorithm and decompression model whose numbers have been detected.

4. A chip card according to Claim 2, comprising a fourth means (MM) for storing a decompression model received previously to a received compressed data field, and the decompression means (PR) detects the number of a decompression algorithm (ALi) preceding the said received field of compressed data so that these are decompressed according to the decompression algorithm whose number has been detected and the decompression model read in the fourth storage means (MM).

5. A chip card according to Claim 2, comprising a fourth means (MM) for storing a decompression model implicitly deduced from a compressed data field during writing in the first storage means (MC), and the decompression means (PR) detects the number of a decompression algorithm (ALi) preceding the said stored field of compressed data so that these are decompressed according to the decompression algorithm whose number was detected and the derived decompression model read in the fourth storage means (MM).

6. A chip card according to any one of Claims 1 to 5, in which the decompression means (PR) detects an indication (CLA: B2, B3) on the compressed or non-compressed state of each received compressed data field so that the decompression means (PR) decompresses the

data only in the data fields preceded by an indication of compressed state.

7. A protocol data unit for being received notably by the chip card according to any one of Claims 1 to 6, comprising a header (ET) and a data field (DATA), the header including the length (LC) of the data field, characterised in that the header (ET) comprises an indication (LDD) on the expected decompressed data length after decompression of the data field (DATA).

8. A protocol data unit according to Claim 7, in which the indication on the expected decompressed data length (LDD) is an n-bit word equal to the expected length of the decompressed data modulo 2^n, the expected length being expressed in decompressed m-bit data words, n being an integer equal to at least 0 and m being an integer equal to at least 1.

9. A protocol data unit according to Claim 7 or 8, in which the header (ET) comprises the number (ALi) of a decompression algorithm by means of which the data compressed in the data field (DATA) are to be decompressed.

10. A protocol data unit according to Claim 9, in which the header (ET) comprises the number (Mij) of a decompression model which corresponds to the decompression algorithm whose number (ALi) is included in the header and by means of which the compressed data in the data field (DATA) are to be decompressed.

11. A protocol data unit according to any one of Claims 7 to 10, in which the header (ET) includes a

data state indication (B1, B2) having a first state (DATA) when the data in the data field are not compressed, and having a second state when the data in the data field (DATA) are compressed.

12. A protocol data unit according to Claim 11, in which the data state indication (B1, B2) has a third state when the data in the data field (DATA) are to be decompressed in accordance with a predetermined decompression algorithm (AL0) and a predetermined decompression model (M00).

13. A protocol data unit according to Claim 11 or 12, in which the header (ET) comprises the number of a decompression algorithm (ALi), the number of a decompression model (Mij) and the indication on the expected decompressed data length (LDD) when the data state indication (B1, B2) is at the second state.

14. A method for decompressing compressed data fields (DATA) to be implemented notably in the chip card according to any one of Claims 1 to 6, each compressed data field being preceded by an indication on the expected decompressed data length (LDD) corresponding to compressed data contained in the field and by a length (LC) of the compressed data contained in the field, characterised by the following steps:

- detecting (D3) the length (LC) of the compressed data and storing (D0) the compressed data field (DATA) over the detected length, and

- detecting (D8) the indication on the expected decompressed data length (LDD) and decompressing (D9)

the data so as to stop the decompression according to the detected indication (LDD).

15. A method according to Claim 14, comprising a step (D6) of selecting a decompression algorithm (ALi) amongst several decompression algorithms (AL0 to ALI) according to the number of an algorithm preceding the compressed data field in order to decompress the data in the field in accordance with the selected decompression algorithm.

16. A method according to Claim 15, comprising a step (D7, D72) of selecting a decompression model (Mij) amongst several decompression models (Mi0 to MiJ) associated with the decompression algorithm selected according to the number of a model preceding the compressed data field in order to decompress the data in the field in accordance with the decompression algorithm selected and the decompression model selected.

17. A method according to Claim 15, comprising a step (D71) of storing a decompression model (Mij) received previously in the compressed data field (DATA) in order to decompress the data in the field in accordance with the selected decompression algorithm and the stored decompression model.

18. A method according to Claim 15, comprising a step (D71) of storing a decompression model (Mij) deduced implicitly from the received compressed data field (DATA) in order to decompress the data in the field in accordance with the selected decompression

algorithm and the deduced and stored decompression model.

19. A method according to any one of Claims 14 to 18, comprising a step (D4, D50, D51, D52) of detecting a data state indication (B2, B3) preceding each decompressed data field in order to decompress the data in the field only when the data state indication is not at a first predetermined state.

20. A method according to Claim 19, according to which the step (D8) of detecting an indication on the expected decompressed data length (LDD) is not performed when the data state indication (B2, B3) is at a predetermined state indicating that the compressed data are to be decompressed according to a predetermined algorithm and model (AL0, M00).

FIG. 1

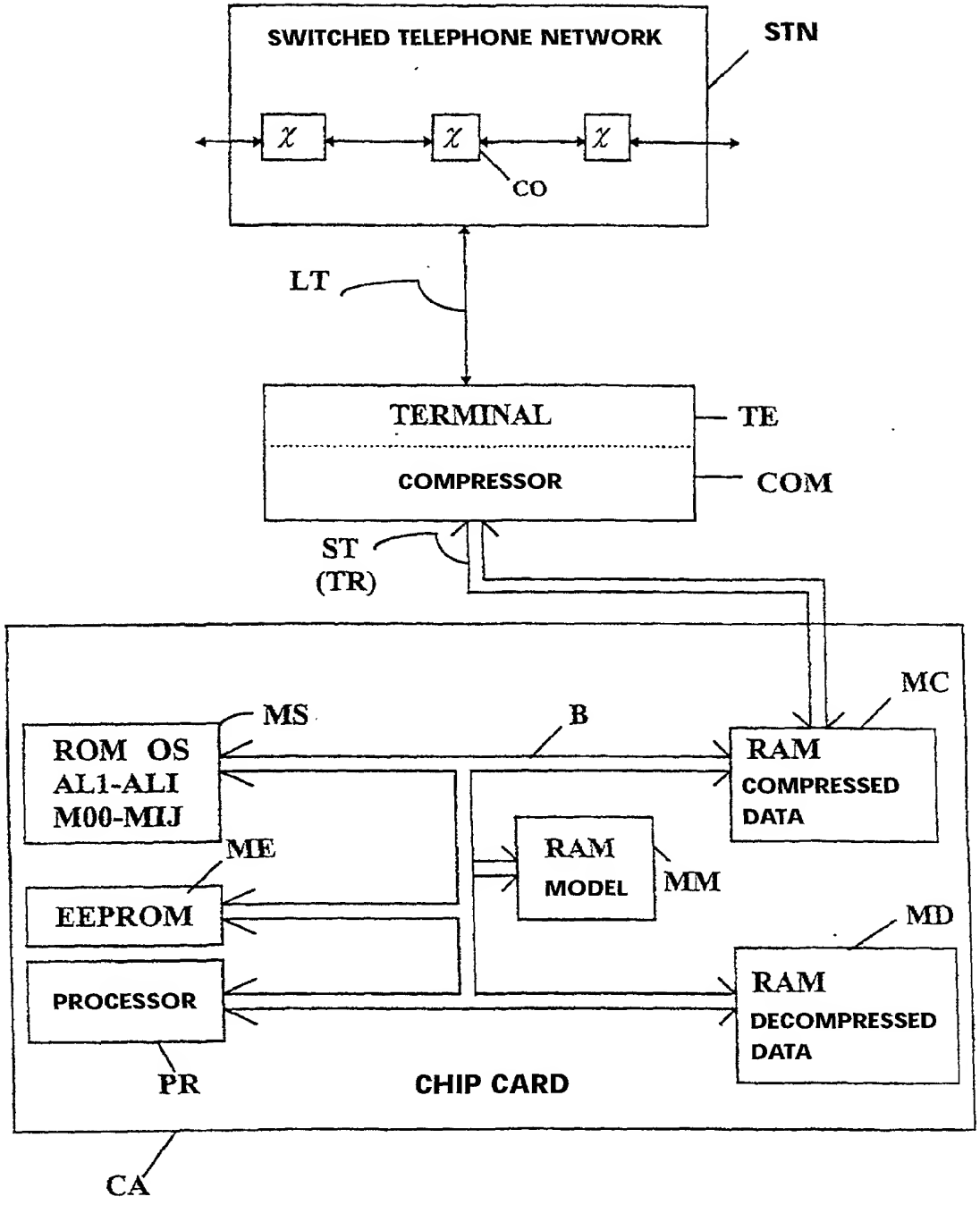

SWITCHED TELEPHONE NETWORK
STN
CO
LT
TERMINAL
TE
COMPRESSOR
COM
ST
(TR)
MC
MS
B
ROM OS
AL1-ALI
M00-MIJ
RAM
COMPRESSED
DATA
ME
RAM
MODEL
MM
EEPROM
MD
PROCESSOR
RAM
DECOMPRESSED
DATA
PR
CHIP CARD
CA

FIG. 2

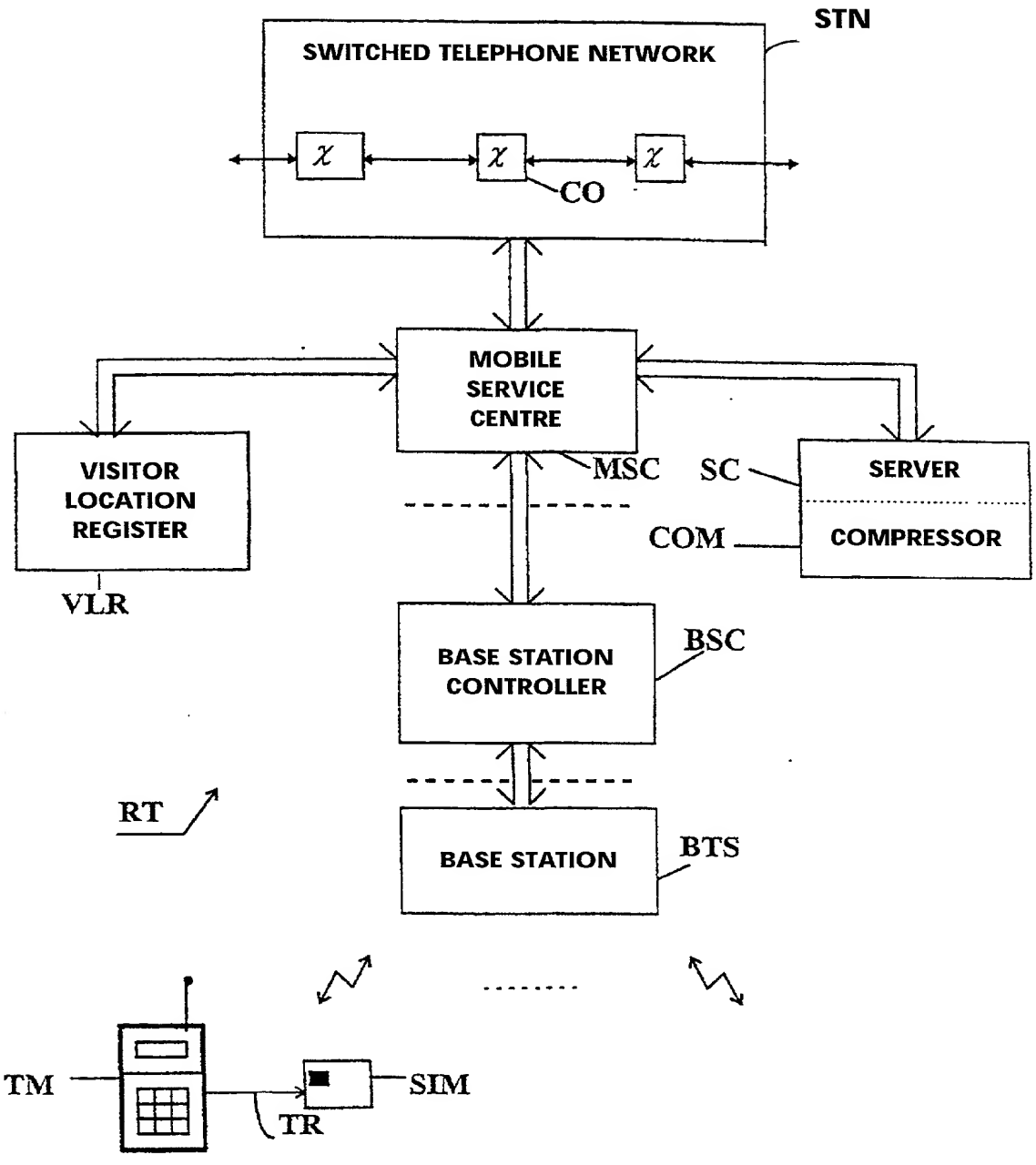

STN
SWITCHED TELEPHONE NETWORK
CO
MOBILE SERVICE CENTRE
MSC
SC
SERVER
COMPRESSOR
COM
VISITOR LOCATION REGISTER
VLR
BASE STATION CONTROLLER
BSC
RT
BASE STATION
BTS
TM
SIM
TR

FIG. 3

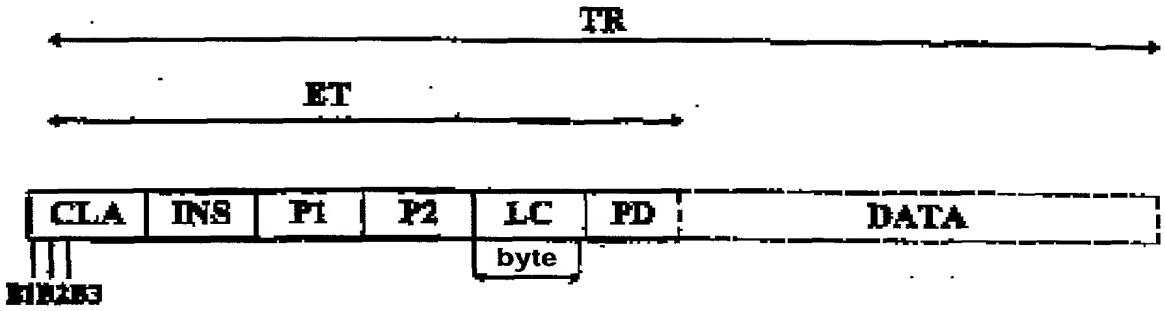

TR
ET
CLA
INS
P1
P2
LC
PD
DATA
byte
B1B2B3

FIG. 4

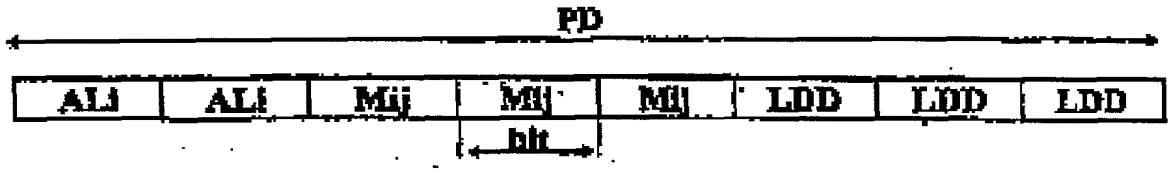

PD
ALi
ALi
Mij
Mij
Mij
LDD
LDD
LDD
bit

FIG. 5

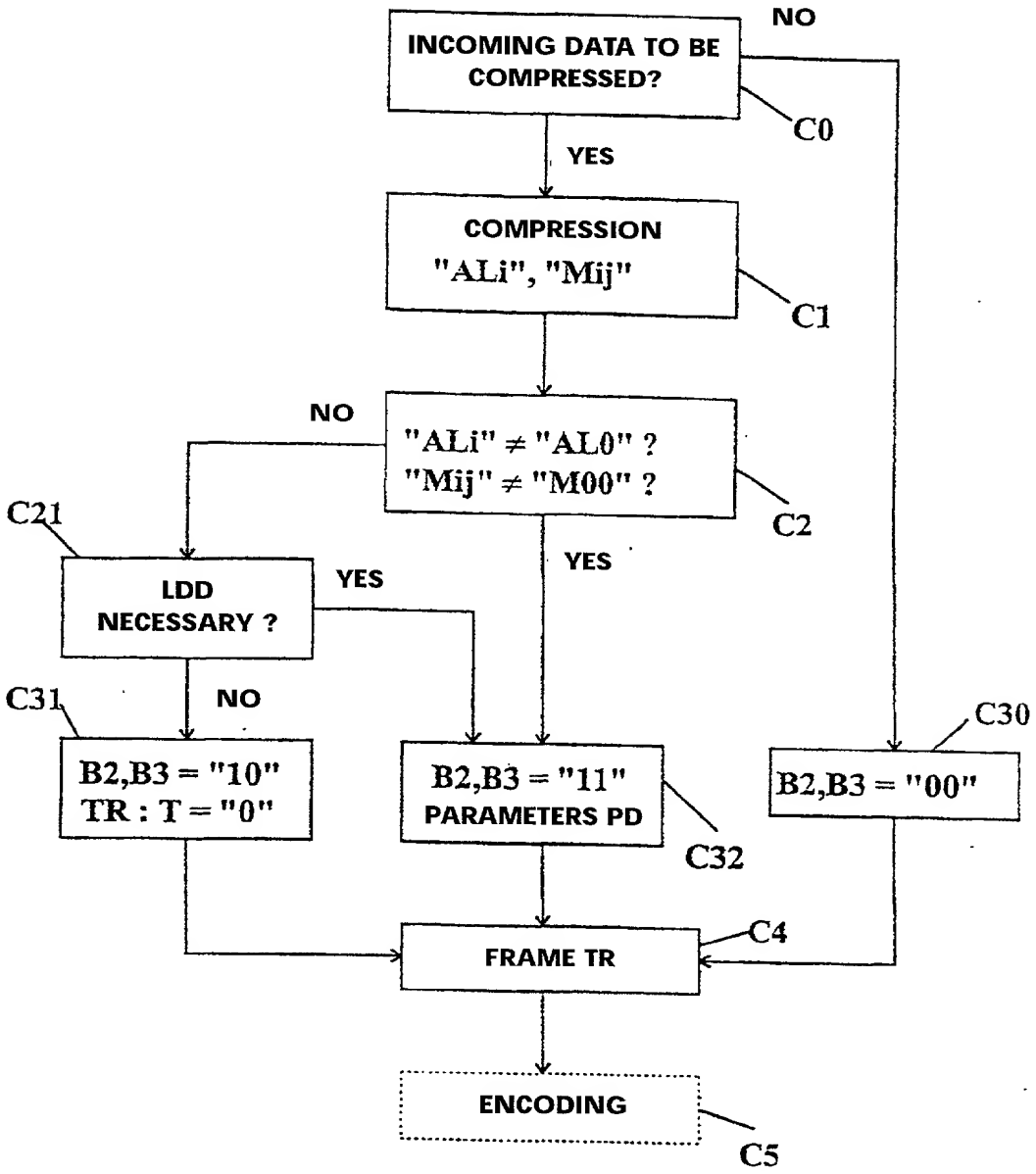
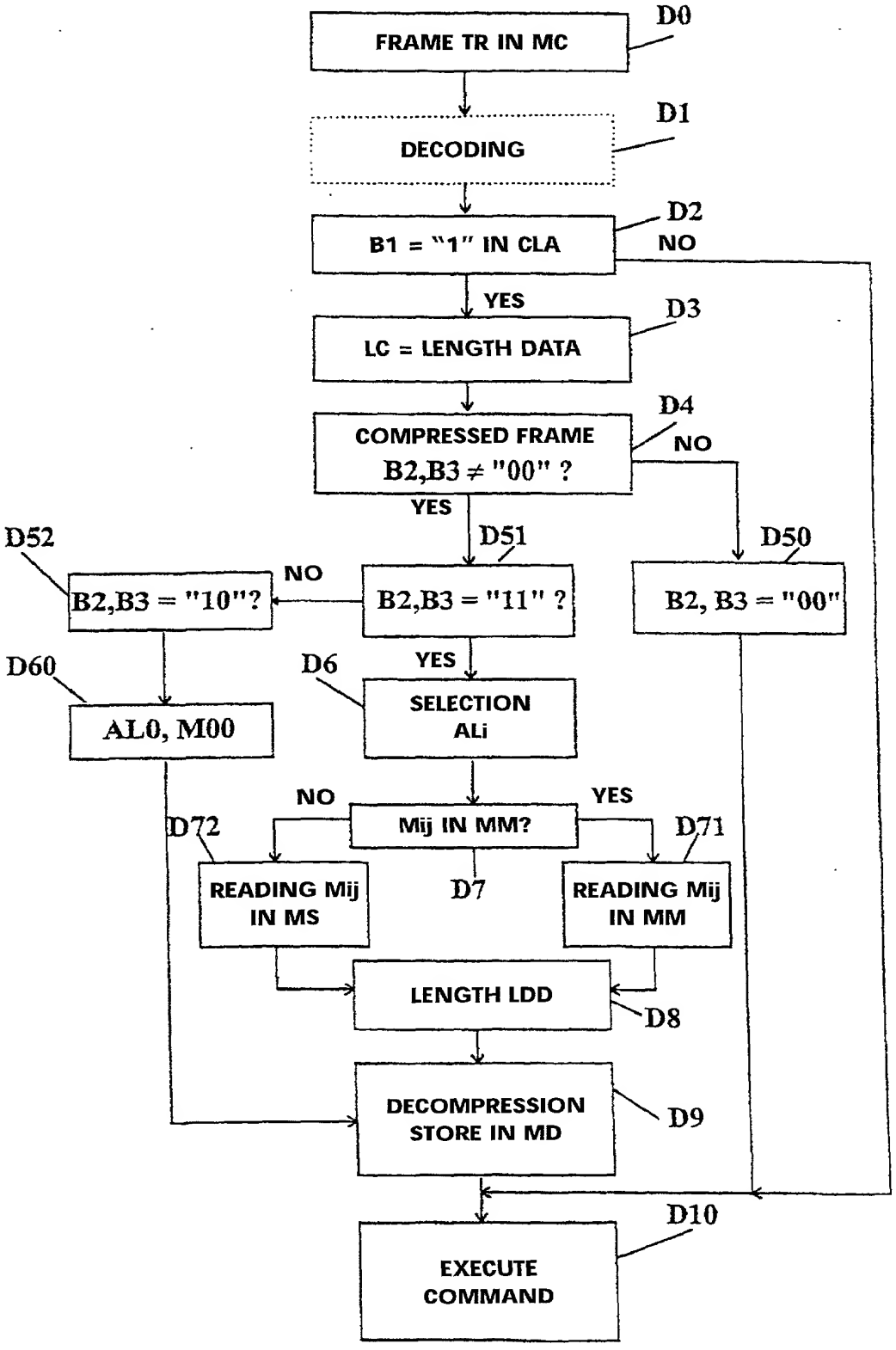

INCOMING DATA TO BE COMPRESSED?
NO
C0
YES
COMPRESSION
"ALi", "Mij"
C1
"ALi" ≠ "AL0" ?
"Mij" ≠ "M00" ?
NO
C2
YES
C21
LDD NECESSARY ?
YES
C31
NO
B2,B3 = "10"
TR : T = "0"
B2,B3 = "11"
PARAMETERS PD
C32
C30
B2,B3 = "00"
C4
FRAME TR
ENCODING
C5

FIG. 6


FRAME TR IN MC
D0
DECODING
D1
B1 = "1" IN CLA
D2
NO
YES
LC = LENGTH DATA
D3
COMPRESSED FRAME
B2,B3 ≠ "00" ?
D4
NO
YES
D52
D51
D50
B2,B3 = "10"?
NO
B2,B3 = "11" ?
B2, B3 = "00"
D60
D6
YES
AL0, M00
SELECTION
ALi
NO
YES
D72
Mij IN MM?
D71
READING Mij
IN MS
D7
READING Mij
IN MM
LENGTH LDD
D8
DECOMPRESSION
STORE IN MD
D9
D10
EXECUTE
COMMAND

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY **(Includes Reference to Provisional and PCT International Applications)**	Attorney's Docket No. 032326-144

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CHIP CARD LOADABLE WITH COMPRESSED DATA

the specification of which (check only one item below):

☐ is attached hereto.

☒ was filed as United States application
Number 09/857,290
on June 1, 2001
and was amended
on _____ (if applicable).

☐ was filed as PCT international application
Number _____
on _____
and was amended
on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(e) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. §119:

COUNTRY (if PCT, indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. §119
France	98/15257	1 December 1998	X Yes _No
			_Yes _No
			_Yes _No
			_Yes _No
			_Yes _No

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

_____ _____
(Application Number) (Filing Date)

_____ _____
(Application Number) (Filing Date)

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (CONT'D) (Includes Reference to Provisional and PCT International Applications)	Attorney's Docket No. 032326-144

I hereby claim the benefit under Title 35, United States Code, §120 of any United States applications(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose to the Office all information known to me to be material to the patentability as defined in Title 37, Code of Federal Regulations §1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. §120:

U.S. APPLICATIONS		STATUS *(check one)*		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.					
PCT APPLICATION NO.	PCT FILING DATE	U.S. APPLICATION NUMBERS ASSIGNED (if any)			
PCT/FR99/-02694	4 November 1999				

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

William L. Mathis	17,337	Eric H. Weisblatt	30,505	Bruce T. Wieder	33,815
Robert S. Swecker	19,885	James W. Peterson	26,057	Todd R. Walters	34,040
Platon N. Mandros	22,124	Teresa Stanek Rea	30,427	Ronni S. Jillions	31,979
Benton S. Duffett, Jr.	22,030	Robert E. Krebs	25,885	Harold R. Brown III	36,341
Norman H. Stepno	22,716	William C. Rowland	30,888	Allen R. Baum	36,086
Ronald L. Grudziecki	24,970	T. Gene Dillahunty	25,423	Brian P. O'Shaughnessy	32,747
Frederick G. Michaud, Jr.	26,003	Patrick C. Keane	32,858	Kenneth B. Leffler	36,075
Alan E. Kopecki	25,813	B. Jefferson Boggs, Jr.	32,344	Fred W. Hathaway	32,236
Regis E. Slutter	26,999	William H. Benz	25,952	Wendi L. Weinstein	34,456
Samuel C. Miller, III	27,360	Peter K. Skiff	31,917	Mary Ann Dillahunty	34,576
Robert G. Mukai	28,531	Richard J. McGrath	29,195		
George A. Hovanec, Jr.	28,223	Matthew L. Schneider	32,814		
James A. LaBarre	28,632	Michael G. Savage	32,596		
E. Joseph Gess	28,510	Gerald F. Swiss	30,113		
R. Danny Huntington	27,903	Charles F. Wieland III	33,096		

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and: _____

Address all correspondence to:

21839

James A. LaBarre
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, Virginia 22313-1404

Address all telephone calls to: James A. LaBarre at (703) 836-6620.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (CONT'D) (Includes Reference to Provisional and PCT International Applications)	Attorney's Docket No. 032326-144

FULL NAME OF SOLE OR FIRST INVENTOR Benoît BRIEUSSEL	SIGNATURE B Brieussel	DATE 1 juillet 2001
RESIDENCE Residence le Variant, 1 Bloc I Appartement 28, Le Charrel, F-13400, Aubagne, FRANCE	CITIZENSHIP FRX FRANCE	
POST OFFICE ADDRESS Residence le Variant, 1 Bloc I Appartement 28, Le Charrel, F-13400, Aubagne, FRANCE		
FULL NAME OF SECOND JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF THIRD JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF FOURTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF FIFTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF SIXTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF SEVENTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF EIGHTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		